Mitigation for single event coupling delay

Selahattin Sayil* and Abhishek B. Akkur

Department of Electrical Engineering, Lamar University, Beaumont, TX 77713, USA

(Received 29 December 2008; final version received 24 February 2009)

With advances in CMOS technology, circuits are increasingly more sensitive to transient pulses caused by single event particles. It has been predicted that the majority of the observed radiation induced soft failures in technologies below 65 nm will be because of transients that will occur in combinational logic (CL) circuits. Researchers mostly considered single event transients as the main source for CL related radiation-induced soft errors. However, for high reliability applications such as avionics additional sources need to be included in reliability analysis. In this work, we report a new error mechanism named ‘Single Event Crosstalk Delay’, investigate the vulnerability of recent technologies to these delay effects and then propose hardening techniques for Single Event Crosstalk Delay. Results are demonstrated using HSpice Simulations with interconnect and device parameters derived in 130, 90 and 65 nm technology.

Keywords: single event effects; crosstalk noise; crosstalk delay; hardening

1. Introduction

The International Technology Roadmap for Semiconductors (2007) has pointed to signal integrity in chips as a major challenge. Transient errors created by ground bounce and IR drop in voltage supply, signal cross-coupling effects, and terrestrial radiation cause reliability issues and compromise the security in unpredictable ways. Nanometer circuits are increasingly becoming more susceptible to interferences coming from these multiple noise sources. Among them, radiation-induced soft errors in commercial nanometer CMOS technologies have recently become a growing concern (Naseer, Draper, Boulghassoul, DasGupta and Witulski 2007).

Terrestrial soft errors in memory have been a very well known problem (Dodd and Massengill 2003). However, because of increasing clock frequencies and shrinking feature sizes soft errors are now affecting CMOS logic. It has been predicted for 45 nm technologies and below, the majority of the observed radiation induced soft failures will be due to transients that will occur in combinational logic (CL) circuits (Mitra, Karnik, Seifert and Zhang 2005). For commercial chips at ground level, soft errors are mainly induced by alpha particles emitted from radioactive decay of uranium and thorium impurities located within the chip packaging and due to atmospheric neutrons. When an energetic radiation particle strikes the sensitive area within a combinational circuit, it loses its energy through...
ionisation and several hole-electron pairs are created. These free carriers can later drift under the electric field, and as a result, a Single Event Transient (SET) voltage pulse is generated. If this pulse can propagate through CL and reaches the storage elements during clock latching window, incorrect data can be stored resulting in soft error. This error is also termed as Single Event Upset (SEU).

Most previous work considered SETs as the main cause for radiation induced CL related soft errors. However, for high reliability applications such as avionics and medical system applications, all other causes for such errors need to be considered simultaneously. These additional error sources include Single Event (SE) Induced Clock Jitters, False Clock Pulses (Seifert, Shipley, Pant, Ambrose and Gill 2005) and SE Crosstalk (Balasubramanian, Sternberg, Bhuva and Massengill 2006).

All these errors occur under specific conditions: SE Clock Jitter occurs when particles inject charge onto clock circuit nodes during clock edge present. An energetic particle strike on clock circuit nodes can also create a ‘False Clock Pulse’ when there is no clock signal present, which can be mistaken for the real clock signal. The SE Crosstalk Noise (Balasubramanian et al. 2006) occurs via interconnect coupling effects.

Researchers mostly ignored CL interconnects in SE Analysis of CMOS circuits. With increasing coupling effects, an SE Transient pulse generated on a circuit node is no longer limited to the logic path existing between the hit node and the latch. The interconnect coupling effects can cause SE Transients to contaminate electronically unrelated circuit paths which can in turn increase the ‘SE Susceptibility’ of CMOS circuits to SETs.

Figure 1 shows aggressor victim pair with its drivers and receivers. Because inputs of both drivers are held at logic 1, the outputs are normally at logic 0. An SE hit at the drain of OFF PMOS transistor of the inverter driver causes output to go to logic 1 for some pulse duration. The SE Transient voltage created can then affect the victim line through coupling capacitor $C_c$ inducing SE Crosstalk noise on the victim.

The cross-coupling effects produced by SE hits can violate noise margins of gates connected to affected line and may result in logic errors. Serious effects may occur if the affected line is somewhat important such as a clock line. Crosstalk noise effects on a clock network may have multiple effects on areas much farther from originating source of the SE Crosstalk point. An upset can be interpreted as a clock edge

![Figure 1. SE crosstalk noise (lumped wire model is for demonstration only).](image-url)
potentially causing many different bits to be stored incorrectly (multiple upsets). In this case, a false clock pulse occurs via coupling mechanism. In addition, Triple-Modular Redundancy (TMR) circuits used to eliminate SE Errors on CL are also susceptible to crosstalk at the inputs of voters (Favalli and Metra 2004; Schrimpf and Fleetwood 2004). This is possible because interconnects between functional units and voters tend to be long and sensitive to crosstalk.

There has been very little work to examine the effect of SE Transients on interconnects. Recent work by Balasubramanian et al. (2006) have studied the crosstalk noise induced by SE Transients for various interconnect lengths and deposited charges using a simple lumped RC model for interconnect. Balasubramanian et al. have shown that SE Transients can produce crosstalk effects on neighbouring lines that can induce logic level state changes for interconnects as small as 100 μm on technologies 90 nm and lower (Balasubramanian et al. 2006). The effect that process technologies have on crosstalk noise pulse has been studied. However, hardening techniques for SE Crosstalk were not examined. To complement the SEU hardening process, coupling effects need to be considered in the SE analysis and hardening of CMOS logic gates because of technology scaling effects that increase both SE vulnerability and crosstalk effects.

Moreover, an SET pulse generated on the affecting wire (because of particle hits on driver transistors) may also cause increased (or decreased) signal delays on neighbouring (victim) lines via cross-coupling effects if victim line driver is in switching. In the example shown in Figure 2, an SEU particle hits the output node of aggressor driver and causes a voltage transient in positive direction. The transient then spreads into the victim line during the switching event via coupling capacitance and cause a signal slowdown as shown on the victim line. The increase in interconnect delay due to the SE Transient coupling can effect circuit performance because delay changes can violate the setup or hold time requirements of logic storage circuits connected to these receivers.

In this work, we report on the SE Induced Crosstalk delay effects for the first time. We investigate the vulnerability of recent technologies to SE induced coupling delay effects using a distributed model for the interconnect. We then propose some hardening techniques to mitigate the SE Crosstalk delay effect. Results are

Figure 2. SE crosstalk delay (lumped wire model is for demonstration only).
demonstrated using HSpice Simulations with interconnect and device parameters derived from ITRS (International Technology Roadmap for Semiconductors 2007) and the Predictive Technology Model (2008), respectively.

2. Analysis of SE induced crosstalk delay and simulation set-up

To compare the SE induced crosstalk delay vs. normal (switching induced) crosstalk delay for newer technologies such as 65 nm, a 10-π model with distributed coupling capacitances is used for every 200 μm of wire to represent the RC distributed behaviour. For the 1 mm wire length chosen in simulations, there were 50-π segments representing the interconnect. Coupling capacitors are also distributed along the line as shown in Figure 3.

We ignore inductance effects and assume that capacitive coupling is the dominant mechanism for crosstalk (Heydari and Pedram 2005; Sayil and Rudrapati 2007).

In all simulations, we consider the interconnect structure shown in Figure 4 with two ground planes. A 1 mm semi-global wire with its neighbour has been considered in 65 nm technology. The interconnect dimensions are taken as follows using the information given in ITRS roadmap (International Technology Roadmap for

Figure 3. Modelling of SE crosstalk delay using a distributed model for interconnect.

Figure 4. The interconnect structure used in simulations.
Semiconductors 2007): The wire width \((W)\) and spacing \((S)\) is taken as 0.14 \(\mu m\), and the wire thickness \(T\) is 0.35 \(\mu m\). We use aggressor and victim driver sizes of 0.54 \(\mu m\)/0.18 \(\mu m\) \((W_p/W_n)\) and assume take the loads at the end of the wires are identically sized inverters. The device parameters were taken from the Predictive Technology Model (2008).

An SE hit was simulated at the output of the aggressor driver using a double exponential current source with a behaviour:

\[
I(t) = \frac{Q}{\tau_a - \tau_p} (e^{-t/\tau_a} - e^{-t/\tau_p})
\]  

where, \(Q\) is the charge (positive or negative) deposited by the particle strike, \(\tau_a\) is the collection time constant of the \(p-n\) junction, \(\tau_p\) is the ion-track establishment time constant. The time constants \(\tau_a\) and \(\tau_p\) are dependent on process technology and taken as 0.2 nS and 0.05 nS, respectively in this work.

The above modelling approach is only approximate. For submicron technologies (above 1 \(\mu m\)), the single event charge due to ion strikes only affected the hit node (i.e. the drain-substrate junction of the hit transistor). However, as we further go into deep submicron technologies such as 65 nm and beyond, a single event strike may affect multiple nodes (nearby devices) and nearby well contacts. As a result, a ‘plateau’ in the single event current pulse following the prompt response will be observed especially with higher LET pulses (Dodd, Shaneyfelt, Felix and Schwank 2004; Benedetto, Eaton, Mavis, Gadlage and Turflinger 2006). Then, the double exponential modelling approach above may not be too accurate. Ideally, a mixed-mode simulator should be used to correctly model SE effects (Dodd et al. 2004).

With mixed-mode simulator approach, some selected components in a circuit is modelled at the device level (i.e. off-biased \(n\)-channel transistor in the struck CMOS inverter) while the rest of the circuit is modelled at the circuit level. One advantage would be the direct calculation of voltage and current pulses induced in the struck device by a given particle strike. However, the limitations of mixed-mode simulator would be the size of the circuit that can be modelled which is usually limited to less than 25 circuit elements and the simulation speed.

Nevertheless, a double exponential current pulse approximation will be used in our simulations to reduce simulation complexity and merely for convenience; as scaling effects and mitigation techniques across various technologies are examined.

To analyse the effect of SE induced crosstalk delay, a rising pulse waveform is applied to victim driver with a 100 ps rise time while aggressor driver is kept at \(V_{DD}\) as shown in Figure 3. An SEU hit charge of 300 fC is simulated at the end of the aggressor driver to examine SE transient effect on victim line delay. To compare this SE induced interconnect delay to the normal aggressor switching induced delay, the SEU current source is removed and then aggressor driver is switched in opposite direction to the victim.

It was previously demonstrated by Kahng, Muddu and Sarto (2000) that aggressor slew rate should be at least two times larger than victim slew rate to have maximum crosstalk delay effect on victim line. Therefore, in this simulation, the aggressor input pulse transition time is chosen as 50 ps to maximise the charge transferred. Figure 5 shows various delays calculated for the ‘\(V_{out}\)’ node shown in Figure 3. The victim line delay without any crosstalk effect (no aggressor switching or SE transient) is taken as reference to calculate the induced delay for each case. It
can be seen that above a certain deposited hit charge, the SETs induce larger delays when compared with the worst case delay induced by regular aggressor switching. Hence, consideration of SE induced coupling delay becomes important in timing analysis. For a 300 fC of deposited charge on the aggressor of a 65 nm technology driver, the delay observed is 287 ps while the normal crosstalk delay when the aggressor switches at 50 ps is observed to be 163 ps.

To observe the effect of scaling on SE coupling delay, a fixed charge of 300 fC has been deposited on 65 nm, 90 nm and 130 nm aggressor drivers separately and the delay at the output has been observed. We observed that the same hit charge causes larger SE induced delays in newer technologies in comparison with previous technologies. Figure 6 shows that a 300 fC deposited charge causes a delay increase of 287 ps in 65 nm technology, while the same charge induces 147 ps in 65 nm technology which is almost the double.

The effect of SE crosstalk delay increases as device sizes further scale down, therefore this effect will become even more important in smaller technologies.

3. Hardening for single event crosstalk delay

Many design techniques have been proposed to mitigate SEU problems in CL. Spatial redundancy techniques such as Triple Modular Redundancy (TMR) method triplicate the CL that is to be protected and uses a voting circuit to filter out the transient (Favalli and Metra 2004; Schrimpf and Fleetwood 2004). In driver sizing technique the gate which drives a set of gates is resized for hardening (Zhou and Mohanram 2006). This increases the critical charge required to produce a SE Transient. Temporal methods sample the data with different delays and produce the output to a voting circuit (Schrimpf and Fleetwood 2004). The voting circuit outputs the majority of the inputs to filter out the glitch. Nevertheless, even these designs leave a vulnerable spot to other SE effects: the interconnect. To control SE induced
crosstalk delay, we investigate the applicability of existing crosstalk noise control techniques in SE Crosstalk delay hardening. The techniques considered are victim driver sizing, wire spacing and wire sizing techniques.

3.1. Victim driver sizing

Victim driver sizing is an effective means to reduce SE crosstalk delay. If the victim driver is sized up, the drive strengths of NMOS and PMOS increases, and as a result, the victim driver switches faster. This effectively reduces the delay effects caused by SE transients on neighbouring wires.

The effect of varying victim driver sizes on SE Crosstalk delay has been observed for 65, 90 and 130 nm technologies as shown in Figure 7. The figure shows the total victim delay (sum of SE induced coupling delay and normal victim delay without

Figure 6. SE crosstalk delay in 65, 90 and 130 nm technologies for a deposited charge of 300 fC.
coupling) with respect to of victim driver size, for a fixed deposited charge of 300 fC on the aggressor driver.

Figure 8 shows the SE induced coupling delay vs. the victim driver size in 65, 90 and 130 nm technologies. From Figure 8, we observe that the SE induced coupling delay decreases in proportion to the increase in victim driver size. For example, the doubling of victim driver size reduces the SE induced delay by 25, 32 and 40% in 65, 90 and 130 nm technologies respectively. Hence, victim driver sizing can effectively reduce the SE induced victim delay.

Although this technique is effective in terms of SE coupling delay mitigation, one might want to also consider the situation where a victim net can also become an aggressor from the opposite standpoint. When the driver of a victim is upsized for reducing delay at the victim net, the noise (hence the delay) it may induce on the
Figure 8. SE crosstalk delay vs. victim driver size in 130, 90 and 65 nm technologies ($Q = 300 \text{ fC}$).

Figure 9. Total victim delay vs. wire spacing in 65, 90 and 130 nm technologies considered (300 fC).
neighbouring aggressor wire will increase because of stronger effect of victim driver. Hence, when a victim driver is upsized, the delay induced on the aggressor line should be checked to make sure no timing violation occurs (Tong Xiao and Malgorzata Marek-Sadowska 2001).

3.2. Wire spacing

For a fixed wire width, if we increase wire spacing to its neighbours, its coupling capacitance decreases while its ground capacitance increases. Considering a parallel plate relation between the wire and its neighbour, there is an inverse relation between the distance \( d \) and the coupling capacitance \( C \). It can be seen that increasing the spacing

![Figure 10. SE crosstalk delay vs. wire spacing in all three technologies (\( Q = 300 \text{ fC} \)).](image)

![Figure 11. SE induced crosstalk delay vs. wire width (300 fC).](image)
between wires increases the ground capacitance of the line. This is because, some electric fields cannot reach the neighbour wire and instead they contribute to the increase in ground capacitance.

Figure 9 shows the effect of spacing ‘S’ on total victim line delay. The simulation is performed with minimum spacing which is defined as $S = W$ ($W$ is the wire width), then the spacing is increased in multiples of $W$. The effect of spacing on total victim line delay is observed for a fixed deposited charge of 300 fC on the aggressor driver. Figure 9 shows that wire spacing technique is very effective in reducing the victim delay in all three technologies.

Figure 10 plots the SE induced crosstalk delay as a function of wire spacing. From this figure it can be observed that, the SE induced crosstalk delay reduces as high as 37, 40 and 46% in 65, 90 and 130 nm technologies, respectively, when wire spacing is doubled.

Result shows that wire spacing is very effective means in reducing SE crosstalk delay however this happens with some large area penalty because of waste of routing resources.

### 3.3. Wire sizing

As a wire width is changed, its resistance and capacitance values also vary. Larger wire sizes mean reduced wire resistances and increased ground capacitances all of which contribute to victim stability. For example, if victim driver is holding the victim line at steady (i.e. GND), it will be more effective holding it because of reduced line resistance and increased capacitances and hence the crosstalk noise induced on victim will be less. However, the same may not be true for SE crosstalk delay.

The effect of wire sizing on SE induced coupling delay is shown in Figures 11 and 12. As one can observe from these figures, wire sizing technique reduces SE induced coupling delay but at the same time, it increases normal victim delay (i.e. in the absence of SE hit) because of increase in ground capacitance.

From the above figures, it can be seen that the rate at which normal victim delay increases is much larger than the rate at which SE induced crosstalk delay decreases. As a result, the total victim delay increases with the increase in wire width. Figure 13 shows the total victim delay vs. wire width in all three technologies considered for a deposited charge of 300 fC.

![Figure 12. Normal (pure) victim delay vs. wire width.](image)
Although wire sizing reduces SE crosstalk delay effect, the total victim wire delay increases as a result of increasing ground, hence this technique cannot be used in controlling the SE induced delay.

4. Conclusion
Advances in technology scaling cause increased coupling effects because of smaller spacing and large thickness to width ratio of interconnects. Most previous research have focussed on the propagation of SET pulses through logic gates without considering interconnects between them. The increase in interconnect delay because of the SE Transient coupling can degrade circuit performance and cause setup or hold time violations. Conventional SEU hardening techniques such as TMR circuits for CMOS logic cannot eliminate SET from spreading to multiple circuit paths due to cross-coupling effects and hence SET crosstalk mitigation needs to be considered.

We have analysed the SE Crosstalk delay effects for recent technologies and shown that increasing SE Crosstalk delay effects occur with smaller technologies.
To complement the current existing SEU hardening techniques for combinational logic, we proposed SE Crosstalk delay hardening techniques for VLSI interconnect. Results are shown using HSpice Simulations with interconnect and device parameters derived from Predictive Technology Model for 65, 90 and 130 nm technologies. Results show that the most effective way to reduce SE crosstalk delay is wire spacing, when area constraints are not important. Victim driver sizing can effectively reduce SE crosstalk delay with some small area penalty. However, the effect of increased victim driver size on aggressor line delay has to be considered for timing purposes. In some cases, however, victim driver sizing technique may need be used in combination with wire spacing if both victim and aggressor noises are comparable to each other.

Acknowledgement
This work was supported in part by the Research Enhancement grant from Lamar University.

References


